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10/648,632	08/25/2003	Yonghua Song	MP0239	4348

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EXAMINER	
NGUYEN, KHANH V	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,632	SONG ET AL.	
	Examiner	Art Unit	
	Khanh V. Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10,12-15,17-21,23-30,32-34,36-43,45 and 46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13,33 and 46* is/are allowed.

6)☒ Claim(s) *1,3-10,12,14,15,17-21,23-30,32,34,36-43 and 45* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 12, 13 and 46 are objected to because of the following informalities:

Claims 12, 13, 45, 46, "a second circuit" should correctly be **-- a circuit --**, since there is no "first circuit" seen in the claims.

Claim 26, "the switch" should correctly be **-- at least one switch --**.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8, 28, 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear what "programmable gain **step**" is intended. "step" is usually involved in method claim only.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-7, 9, 10, 14, 15, 17, 19, 21, 23-27, 29, 30, 34, 36-40, 42, 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Burger, Jr. et al. (5,412,346).

Regarding claims 1, 14, 34, Burger, Jr. et al. (Fig. 6) disclose a variable gain amplifier comprising: an amplifier (120) can be read as a gain stage; transistors (450, 452) operable as switches in parallel with a resistive element (151) can be read as a programmable resistance; and an output node coupled to positive (+) VOUT between the gain stage (120) and the programmable resistance (450, 452, 151), wherein the plurality of switches are operable to change a gain at the output node by opening and closing of switches.

Regarding claims 3, 36, wherein first gain value and second gain value is inherently seen when switch is closed and opened, respectively.

Regarding claims 4, 5, 15, 37, 38, Burger, Jr. et al. (Fig. 6) disclose a variable gain amplifier comprising: an amplifier (120) can be read as a gain stage; transistors (450, 452) operable as switches in parallel with a resistive element (151) can be read as a programmable resistance; and an output node coupled to positive (+) VOUT between the gain stage (120) and the programmable resistance (450, 452, 151), wherein the plurality of switches are operable to change a gain at the output node by opening and closing of switches and at least one switch (452) operable as a variable resistance.

Regarding claims 6, 39, wherein first gain value and second gain value is inherently seen when switch is closed and opened, respectively.

Regarding claims 7, 40, wherein the first resistance value is source-drain resistance of the switch (450, 452).

Regarding claims 9, 42, wherein amplifier (120) is a differential amplifier, thus inherently seen having a differential transistor pair, each transistor can be read as a gain stage for an upper branch (151, 250, 452) and lower branch (4501, 4521, 161).

Regarding claims 10, 30, 43, wherein switches (452, 4521) from upper branch and lower branch operative to be activated and deactivated simultaneously, since they both coupled to a common control voltage (VC1).

Regarding claims 17, 19, wherein voltage (Vin+) can be read as a reference voltage, resistor (131) and capacitor (141) together can be read as a first circuit.

Regarding claim 21, Burger, Jr. et al. (Fig. 6) disclose a variable gain amplifier comprising: voltage (Vin+), capacitor (141), resistor (131) can be read as a first circuit; output voltage (VOUT) can be read as a second circuit; an amplifier circuit can be read as a voltage buffer comprising a gain stage (120); transistors (450, 452) operable as switches in parallel with a resistive element (151) can be read as a programmable resistance; and an output node coupled to positive (+) VOUT between the gain stage (120) and the programmable resistance (450, 452, 151), wherein the plurality of switches are operable to change a gain at the output node by opening and closing of switches.

Regarding claims 23, wherein first gain value and second gain value is inherently seen when switch is closed and opened, respectively.

Regarding claims 24, 25, Burger, Jr. et al. (Fig. 6) disclose a variable gain amplifier comprising: voltage (Vin+), capacitor (141), resistor (131) can be read as a first circuit; output voltage (VOUT) can be read as a second circuit; an amplifier circuit can be read as a voltage buffer comprising a gain stage (120); transistors (450, 452) operable as switches in parallel with a resistive element (151) can be read as a programmable resistance; and an output node coupled to positive (+) VOUT between the gain stage (120) and the programmable resistance (450, 452, 151), wherein the plurality of switches are operable to change a gain at the output node by opening and closing of switches and at least one switch (452) operable as a variable resistance.

Regarding claims 26, wherein first gain value and second gain value is inherently seen when switch is closed and opened, respectively.

Regarding claim 27, wherein the first resistance value is source-drain resistance of the switch (450, 452).

Regarding claim 29, wherein amplifier (120) is a differential amplifier, thus inherently seen having a differential transistor pair, each transistor can be read as a gain stage for an upper branch (151, 250, 452) and lower branch (4501, 4521, 161).

Regarding claim 30, 43 wherein switches (452, 4521) from upper branch and lower branch operative to be activated and deactivated simultaneously, since they both coupled to a common control voltage (VC1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 18, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burger, Jr. et al.

Regarding claims 18, 20, Burger, Jr. et al. disclose the claimed invention except a second circuit is a load circuit. However, it is well known in the art that amplifier circuit must have an output load, see Fig. 2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3-7, 9, 12, 14, 15, 17-21, 23-27, 29, 32, 34, 36-42, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lau et al. (6,462,588).

Regarding claims 1, 14, 34, Lau et al. disclose the claimed invention except a resistive element in parallel with plurality of switches. Lau et al. (Fig. 4) disclose an amplifier circuit comprising: transistor pair (194, 196) can be configured as a gain stage; a plurality of switching pairs ((186, 188) and (190, 192)) in parallel with transistors (182 and 184), respectively, wherein transistors (182, 184) each has an associated resistance, thus functional equivalent as claimed resistive element together with the switching pairs can be read as a programmable resistance; an output node coupled between the gain stage (194, 196) and the programmable resistance ((182, 186, 188) and (184, 190, 192)), wherein the switches ((186, 188) and (190, 192)) can be configured to change a gain at the output node by switching the switches on/off.

Regarding claims 3, 36, 38, wherein the gain at he output node has a first gain value when the switches are activated (ON) and second value when the switches are configured in OFF mode/deactivated.

Regarding claims 4, 15, 37, Lau et al. disclose the claimed invention except a resistive element in parallel with plurality of switches. Lau et al. (Fig. 4) disclose an amplifier circuit comprising: transistor pair (194, 196) can be configured as a gain stage; a plurality of switching pairs ((186, 188) and (190, 192)) in parallel with transistors (182 and 184), respectively, wherein transistors (182, 184) each has an associated resistance, thus functional equivalent as claimed resistive element together with the switching pairs can be read as a programmable resistance; an output node coupled between the gain stage (194, 196) and the programmable resistance ((182, 186, 188) and (184, 190, 192)), wherein the switches ((186, 188) and (190, 192)) can be configured to change a gain at the output node by switching the switches on/off and at least one switch (186/188) can be used as a variable resistance.

Regarding claims 5, 38, wherein the gain at he output node has a first gain value when the switches are activated (ON) and second value when the switches are configured in OFF mode/deactivated.

Regarding claims 6, 39, the switches (186, 188, 190, 192) each has an associated resistance which can be read as a first resistance value when activated an no resistance value when deactivated.

Regarding claims 7, 40, wherein the first resistance value is source-drain of the switch (186, 188, 190, 192)

Regarding claims 9, 42, wherein transistors (182, 186, 188, 194) can be one branch and transistors (184, 190, 192, 196) can be read as another branch.

Regarding claims 12, 17, 18, 45, Lau et al. (Fig. 3) disclose a driver circuit (150), which can be read as claimed circuit/first/second circuit having the function thereof, wherein the voltage input to the driver (150) can be read as a reference voltage.

Regarding claims 18, 20, wherein output signal from gain stage is coupled to further amplifier (200), which coupled to some load.

Regarding claim 21, Lau et al. disclose the claimed invention except a resistive element in parallel with plurality of switches. Lau et al. (Figs. 3, 4) disclose an amplifier circuit comprising: a driver circuit (150) can be read as a first circuit; a second circuit 200); transistor pair (194, 196) can be configured as a gain stage; a plurality of switching pairs ((186, 188) and (190, 192)) in parallel with transistors (182 and 184), respectively, wherein transistors (182, 184) each has an associated resistance, thus functional equivalent as claimed resistive element together with the switching pairs can be read as a programmable resistance; an output node coupled between the gain stage (194, 196) and the programmable resistance ((182, 186, 188) and (184, 190, 192)), wherein the switches ((186, 188) and (190, 192)) can be configured to change a gain at the output node by switching the switches on/off.

Regarding claim 23, wherein the gain at he output node has a first gain value when the switches is activated (ON) and second value when the switches is configured in OFF mode/deactivated.

Regarding claim 24, Lau et al. disclose the claimed invention except a resistive element in parallel with plurality of switches. Lau et al. (Figs. 3, 4) disclose an amplifier circuit comprising: a driver circuit (150) can be read as a first circuit; a second circuit 200); transistor pair (194, 196) can be configured as a gain stage; a plurality of switching pairs ((186, 188) and (190, 192)) in parallel with transistors (182 and 184), respectively, wherein transistors (182, 184) each has an associated resistance, thus functional equivalent as claimed resistive element together with the switching pairs can be read as a programmable resistance; an output node coupled between the gain stage (194, 196) and the programmable resistance ((182, 186, 188) and (184, 190, 192)), wherein the switches ((186, 188) and (190, 192)) can be configured to change a gain at the output node by switching the switches on/off and at least one switch (186/188) can be used as a variable resistance.

Regarding claim 25, wherein the gain at he output node has a first gain value when the switches is activated (ON) and second value when the switches is configured in OFF mode/deactivated.

Regarding claim 26, the switches (186, 188, 190, 192) each has an associated resistance which can be read as a first resistance value when activated an no resistance value when deactivated.

Regarding claim 27, wherein the first resistance value is source-drain of the switch (186, 188, 190, 192)

Regarding claim 29, wherein transistors (182, 186, 188, 194) can be one branch and transistors (184, 190, 192, 196) can be read as another branch.

Regarding claim 32, Lau et al. (Fig. 3) disclose a driver circuit (150), which can be read as claimed third circuit having the function thereof.

Allowable Subject Matter

Claims 13, 33, 46 allowed.

Claims 13, 33, 46 call for, among others, a circuit to control an accuracy of the gain comprising: a reference resistive element; a tunable resistive element having the functions and connections as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh V. Nguyen whose telephone number is (571) 272-1767. The examiner can normally be reached from 8:00 AM - 3:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KHANH VAN NGUYEN
PRIMARY EXAMINER
Art Unit: 2817